

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LCX16373AFT

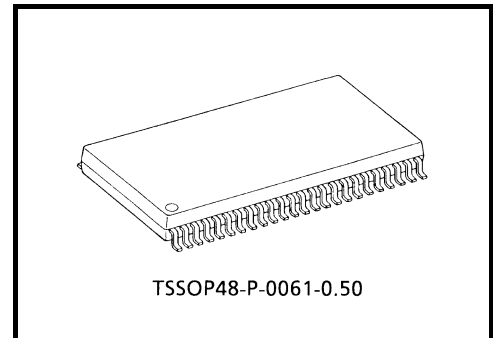
## Low-Voltage 16-Bit D-Type Latch with 5-V Tolerant Inputs and Outputs

The TC74LCX16373AFT is a high-performance CMOS 16-bit D-type latch. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the  $\overline{OE}$  input is high, the outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

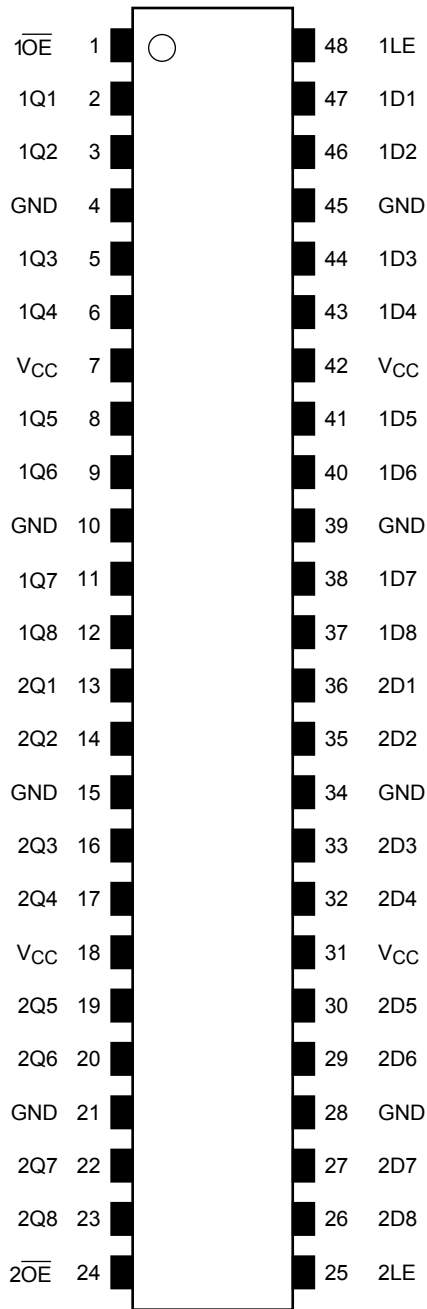


Weight: 0.25 g (typ.)

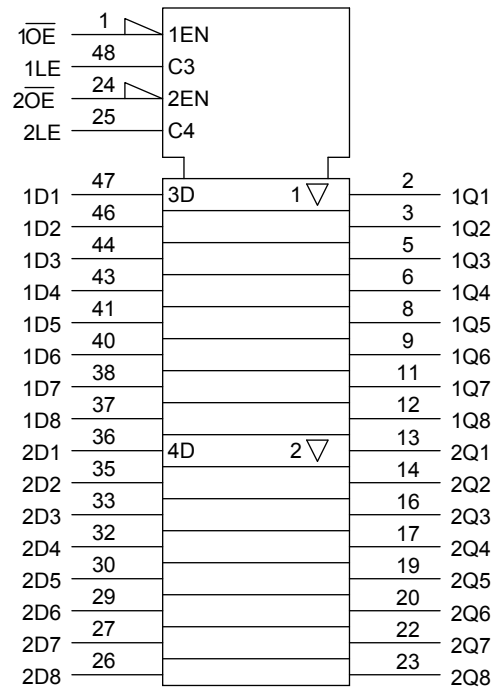
### Features

- Low-voltage operation:  $V_{CC} = 2.0$  to  $3.6$  V
- High-speed operation:  $t_{pd} = 7.0$  ns (max) ( $V_{CC} = 3.0$  to  $3.6$  V)
- Output current:  $|I_{OH}|/I_{OL} = 24$  mA (min) ( $V_{CC} = 3.0$  V)
- Latch-up performance:  $\pm 500$  mA
- Package: TSSOP (thin shrink small outline package)
- Power-down protection provided on all inputs and outputs

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

Inputs			Outputs
$\overline{1OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

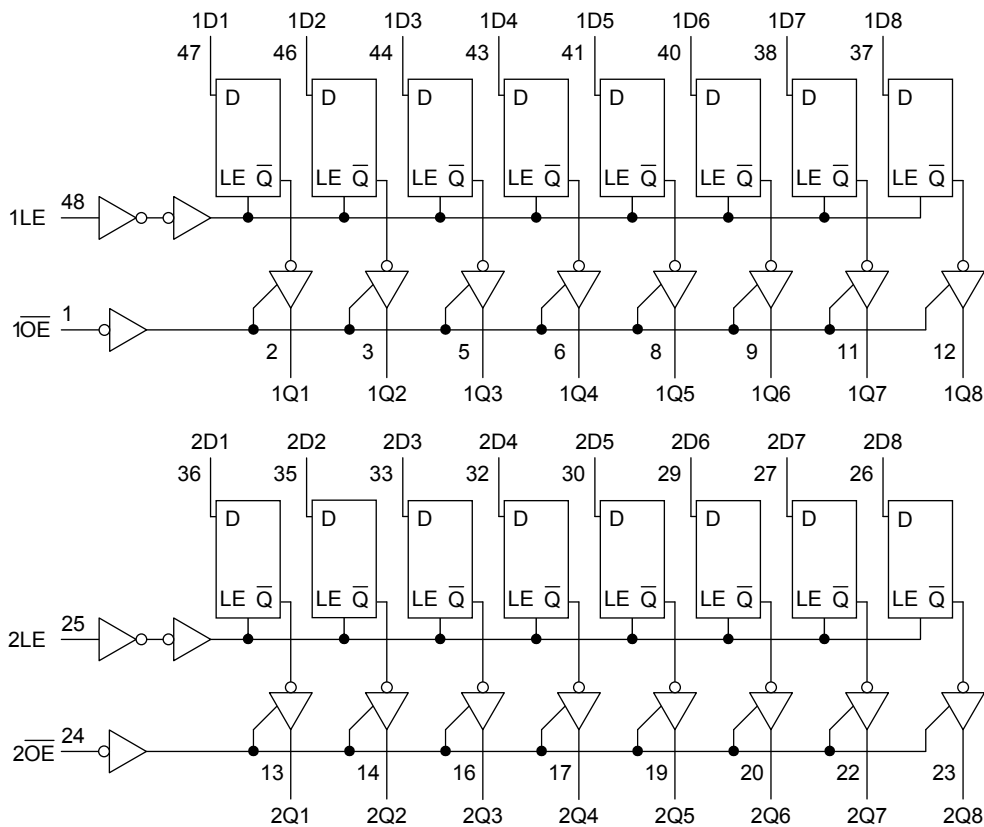
Inputs			Outputs
$\overline{2OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 7.0	V
Input voltage	$V_{IN}$	-0.5 to 7.0	V
Output voltage	$V_{OUT}$	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 4)	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	400	mW
DC $V_{CC}$ /ground current per supply pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: Output in OFF state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Recommended Operating Conditions (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	2.0 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to 5.5 (Note 3)	V
		0 to $V_{CC}$ (Note 4)	
Output current	$I_{OH}/I_{OL}$	$\pm 24$ (Note 5)	mA
		$\pm 12$ (Note 6)	
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	$dt/dv$	0 to 10 (Note 7)	ns/V

Note 1: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5:  $V_{CC} = 3.0$  to  $3.6$  V

Note 6:  $V_{CC} = 2.7$  to  $3.0$  V

Note 7:  $V_{IN} = 0.8$  to  $2.0$  V,  $V_{CC} = 3.0$  V

## Electrical Characteristics

### DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.7 to 3.6	2.0	—	V
	L-level	V <sub>IL</sub>	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12 mA	2.7	2.2	—	
				I <sub>OH</sub> = -18 mA	3.0	2.4	—	
				I <sub>OH</sub> = -24 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7 to 3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	—	20.0	μA
			V <sub>IN</sub> /V <sub>OUT</sub> = 3.6 to 5.5 V		2.7 to 3.6	—	±20.0	
Increase in I <sub>CC</sub> per input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7 to 3.6	—	500	

## AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time (D-Q)	t <sub>pLH</sub>	Figure 1, Figure 2	2.7	—	8.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	7.0	
Propagation delay time (LE-Q)	t <sub>pLH</sub>	Figure 1, Figure 2	2.7	—	8.0	ns
	t <sub>pHL</sub>		3.3 ± 0.3	1.5	7.0	
3-state output enable time	t <sub>pZL</sub>	Figure 1, Figure 3	2.7	—	8.2	ns
	t <sub>pZH</sub>		3.3 ± 0.3	1.5	7.2	
3-state output disable time	t <sub>pLZ</sub>	Figure 1, Figure 3	2.7	—	8.2	ns
	t <sub>pHZ</sub>		3.3 ± 0.3	1.5	7.2	
Minimum pulse width (LE)	t <sub>w</sub> (H)	Figure 1, Figure 2	2.7	4.0	—	ns
			3.3 ± 0.3	3.0	—	
Minimum setup time	t <sub>s</sub>	Figure 1, Figure 2	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum hold time	t <sub>h</sub>	Figure 1, Figure 2	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output to output skew	t <sub>osLH</sub>	(Note)	2.7	—	—	ns
	t <sub>osHL</sub>		3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.  
 (t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)

## Dynamic Switching Characteristics

(Ta = 25°C, input: t<sub>r</sub> = t<sub>f</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

## Capacitive Characteristics (Ta = 25°C)

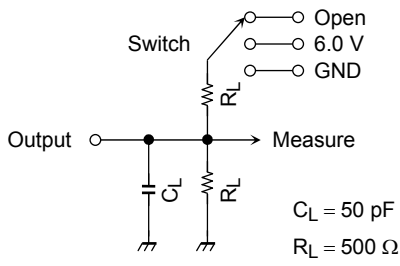
Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit	
Input capacitance	C <sub>IN</sub>	—	3.3	7	pF	
Output capacitance	C <sub>OUT</sub>	—	3.3	8	pF	
Power dissipation capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz	(Note)	3.3	25	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

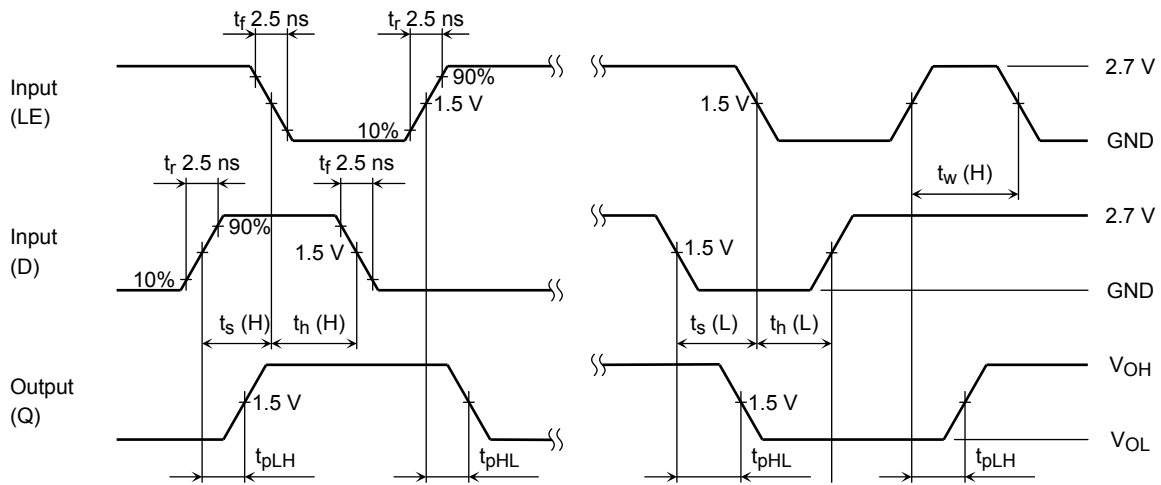
**AC Test Circuit**



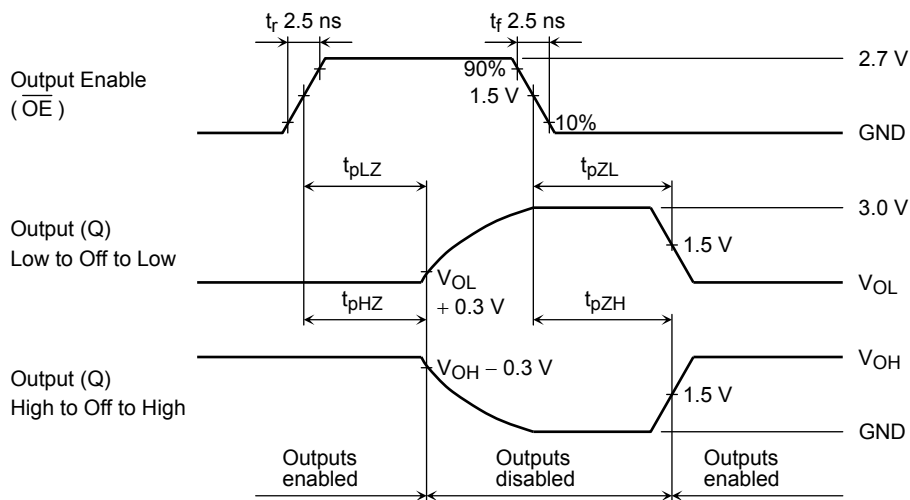
Parameter	Switch
$t_{pLH}, t_{pHL}$	Open
$t_{pLZ}, t_{pZL}$	6.0 V
$t_{pHZ}, t_{pZH}$	GND
$t_w, t_s, t_h$	Open

**Figure 1**

**AC Waveform**



**Figure 2  $t_{pLH}, t_{pHL}, t_w, t_s, t_h$**

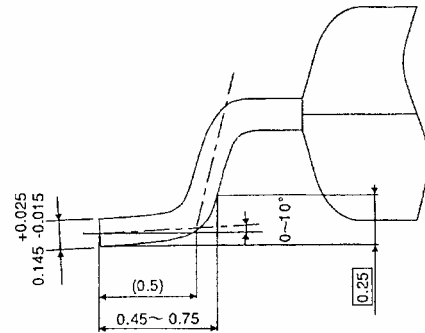
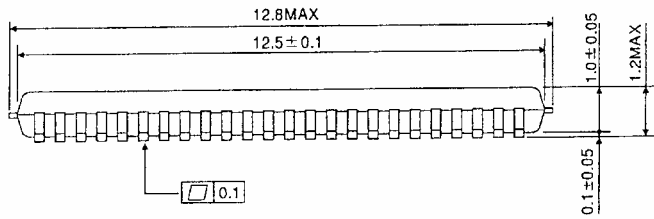
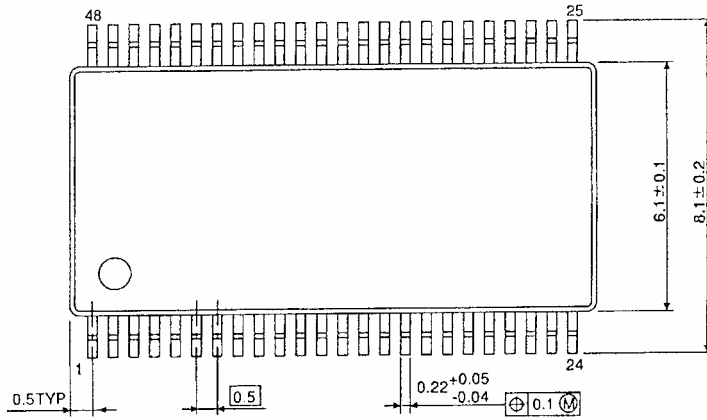


**Figure 3  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$**

**Package Dimensions**

TSSOP48-P-0061-0.50

Unit : mm



Weight: 0.25 g (typ.)



**Note: Lead (Pb)-Free Packages****TSSOP48-P-0061-0.50****RESTRICTIONS ON PRODUCT USE**

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